**LAB 8**

**Active low/high Enabling Decoder and Priority Encoder**

Name.

Reg. No.

**Equipment/Components**

**Software:** Circuit Maker

**Description**

**Enabling**

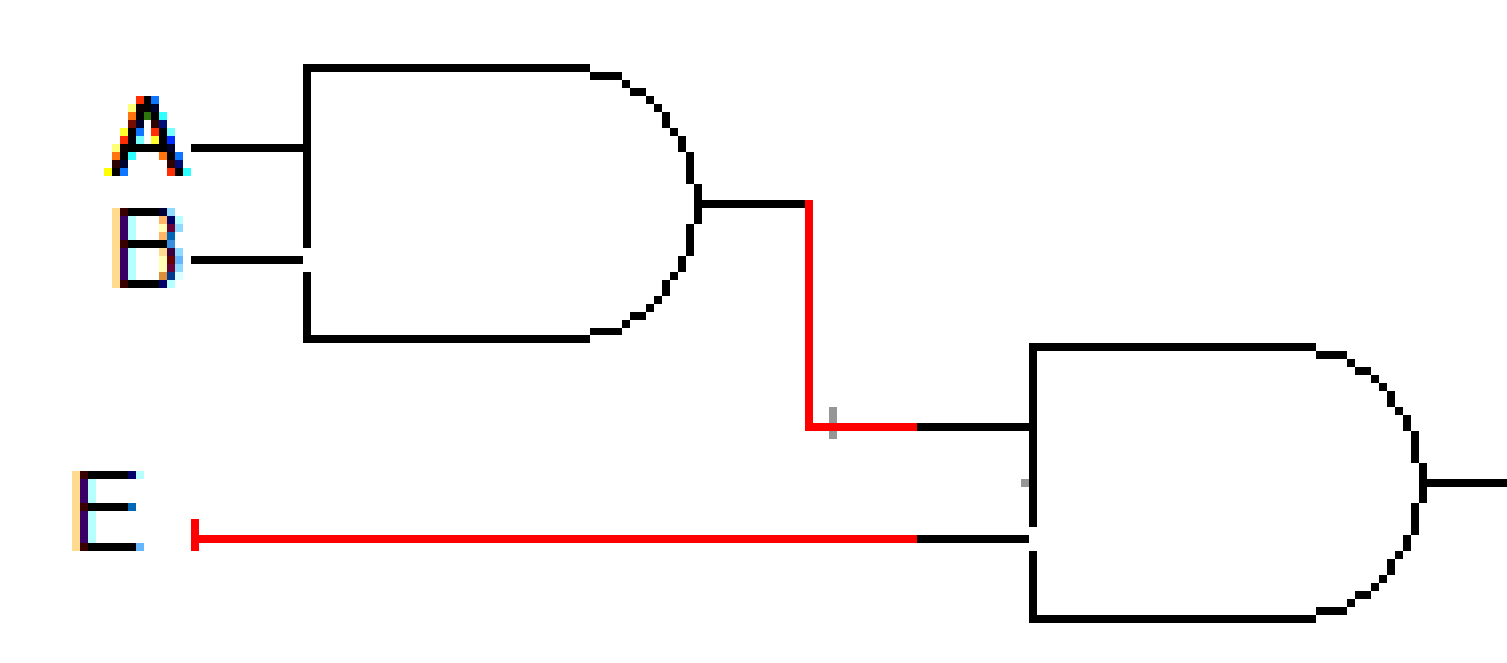
The concept of enabling is to permit an input signal to pass through or is blocked completely. The enable bit is also used to enable or disable the normal functioning of a logic circuit. A logic circuit can be enabled or disabled using a single enable bit. This enable bit can be either active low or active high. Let us have an example of an AND gate with enable bit. If the enable bit is active high then it means that the AND gate performs normal operation if the enable bit is one else the output of AND gate is forced to be zero.

If the enable bit is active low then it means that the AND gate performs normal operation if the enable bit is zero else the output of AND gate is forced to be zero.

**Table 1: Truth Table for Active high enabling**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | | | | **Output** |
| **E** | **A** | **B** |  | |
| 0 | X | X | 0 | |
| 1 | 0 | 0 | 0 | |
| 1 | 0 | 1 | 0 | |
| 1 | 1 | 0 | 0 | |
| 1 | 1 | 1 | 1 | |

**Circuit Diagram**

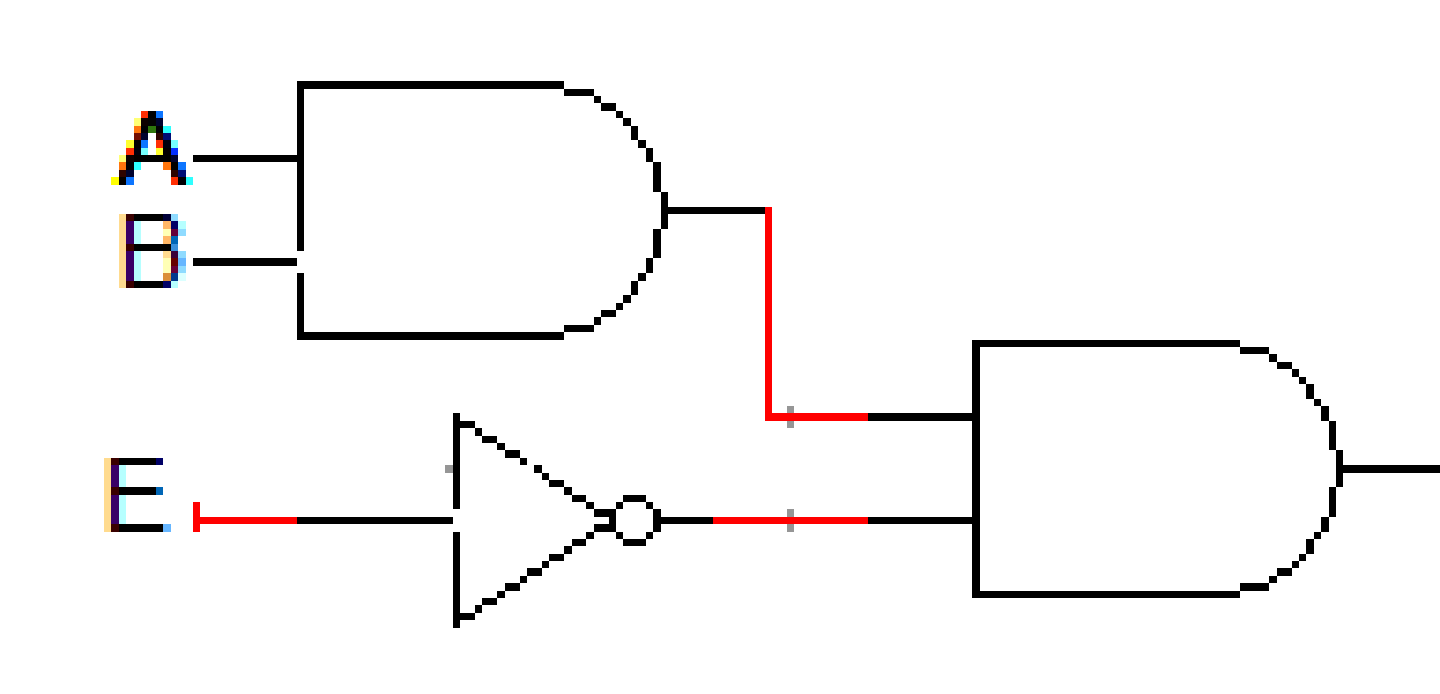


**Figure 1: Active high enabling**

**Table 2: Truth Table for Active low enabling**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Inputs** | | | | **Output** |
| **E** | **A** | **B** |  | |
| 1 | X | X | 0 | |
| 0 | 0 | 0 | 0 | |
| 0 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 0 | |
| 0 | 1 | 1 | 1 | |

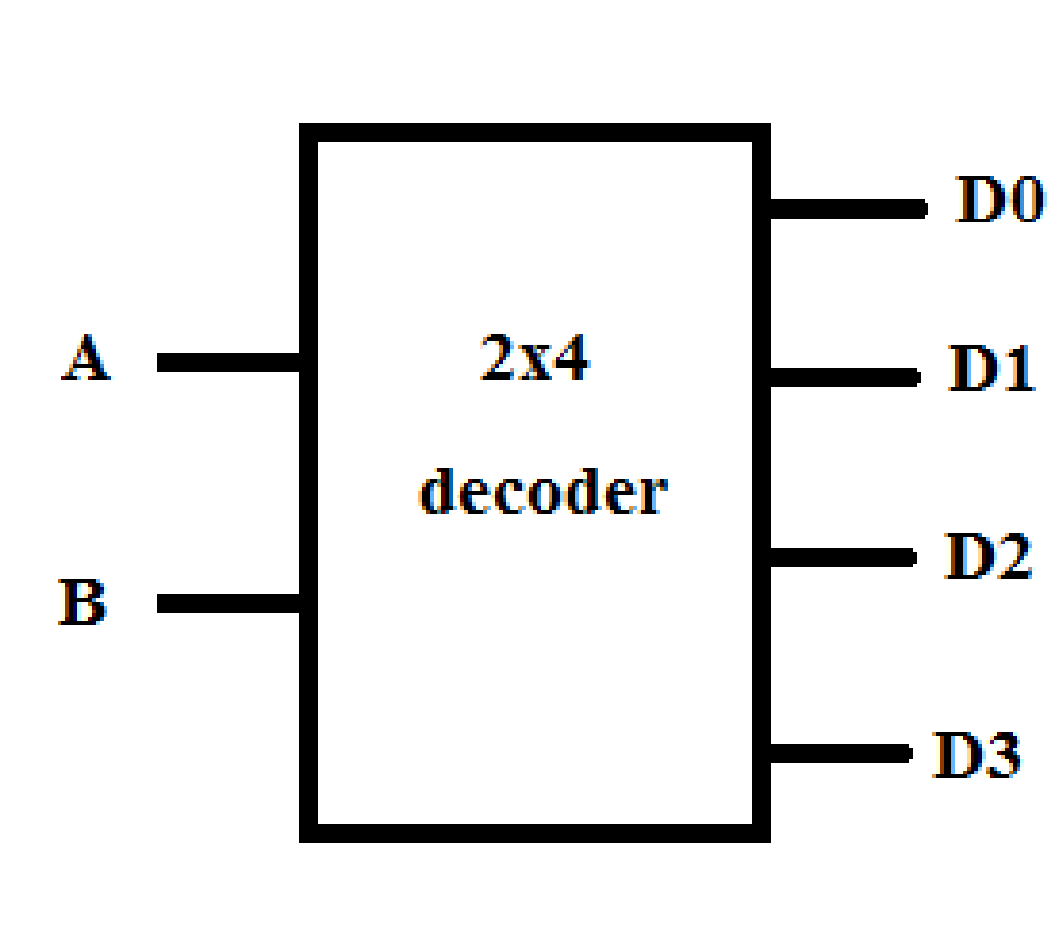
**Circuit Diagram**



**Figure 2: Active low enabling**

**Decoder**

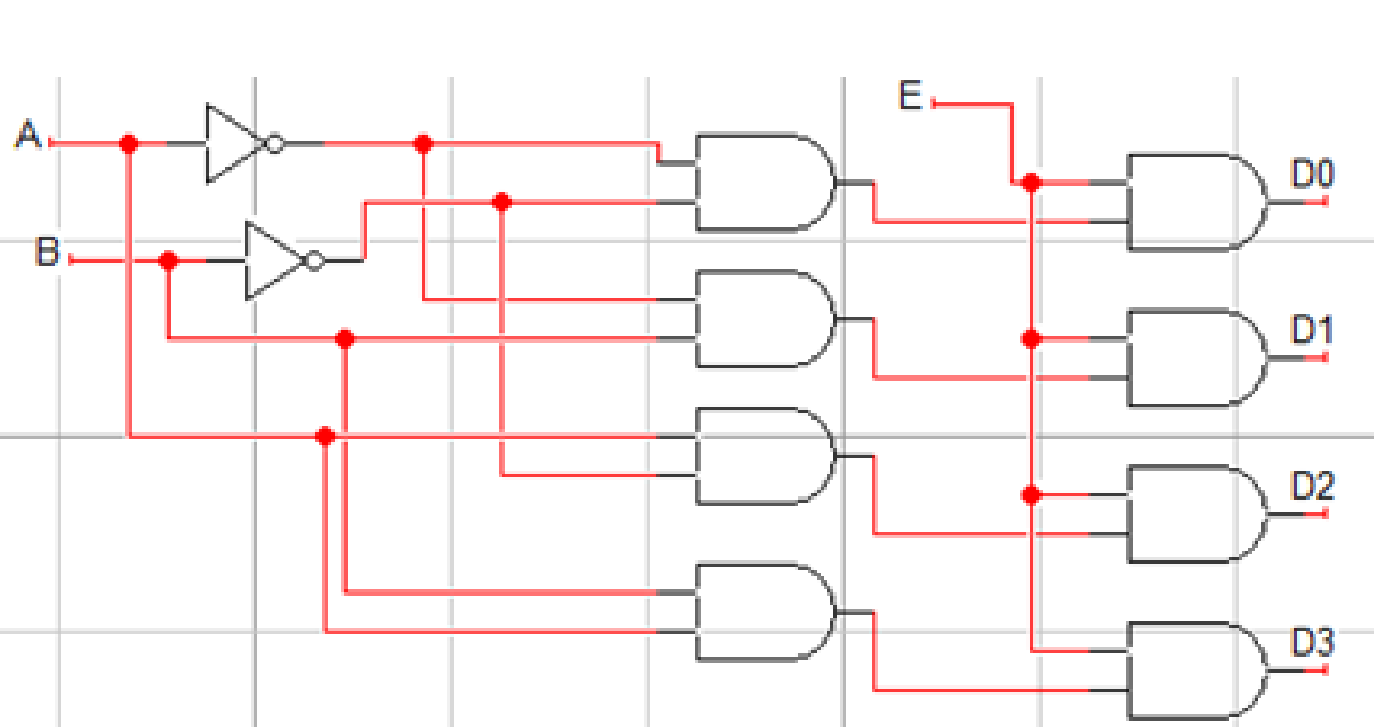
A decoder is a combinational circuit that decodes the coded inputs. A binary decoder has ***n*** inputs and a maximum of ***2n*** outputs. An n-bit binary number provides ***2n*** min terms or max terms. The decoder indicates one of the ***2n*** min terms or max terms at the outputs based on the input combinations. The decoder that produces ***2n*** min terms as its outputs is said to be a decoder with active high outputs, whereas, the decoder that produces ***2n*** max terms as its outputs is said to be a decoder with active low outputs. Let us take ***n***=2 as an example, so that we obtain the 2-to-4 line decoder with active high outputs. Figure below shows the block diagram of 2x4 decoder.



**Figure 3 Decoder**

**Table 3 Active high decoder outputs**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | **Outputs** | | | | |
| **A** | **B** | | **D0** | **D1** | **D2** | **D3** |
| 0 | 0 | | 1 | 0 | 0 | 0 |
| 0 | 1 | | 0 | 1 | 0 | 0 |
| 1 | 0 | | 0 | 0 | 1 | 0 |
| 1 | 1 | | 0 | 0 | 0 | 1 |

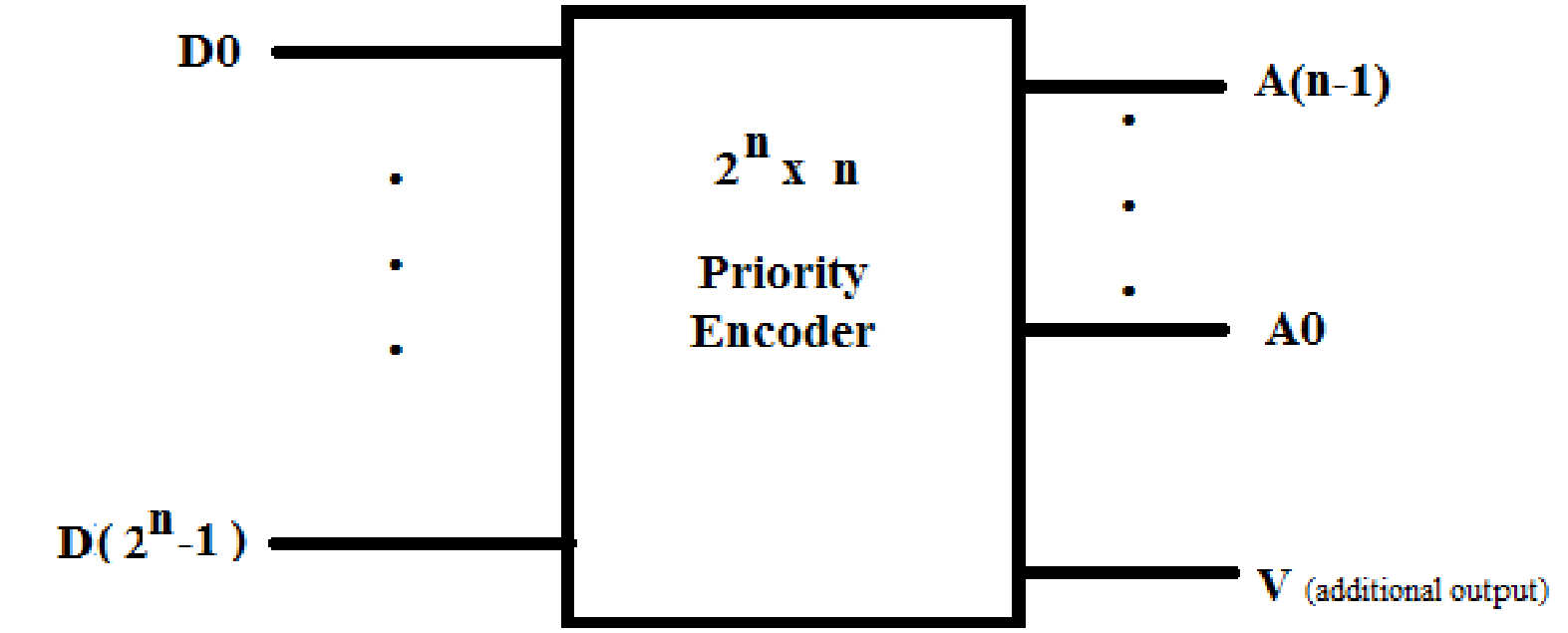
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**Figure 4: Circuit diagram for 2x4 decoder with active high outputs and active high enable**

**Encoder:**

An encoder is a combinational circuit that performs the inverse operation of a decoder. An encoder has a maximum of ***2n*** input lines and ***n*** output lines. The encoder generates binary code at its output lines that represents which input line is active at a given time. In encoder, it is assumed that only one input is active high at a time, if more than one inputs are high simultaneously then ambiguous output is generated. In order to resolve this ambiguity, there must be some input priority function to ensure that only one input is encoded at a time.

A priority encoder is a combinational circuit that encodes the input using priority function i.e. if more than one inputs are high simultaneously than the input having the highest priority will take precedence. Each input line is assigned priority. The most significant input line may be given highest priority and least significant input line the lowest or vice versa. The priority encoder has an additional output to ensure that at least one input line is active high and the binary code at the output lines is valid. Figure shows the block diagram of **2nxn** encoder.



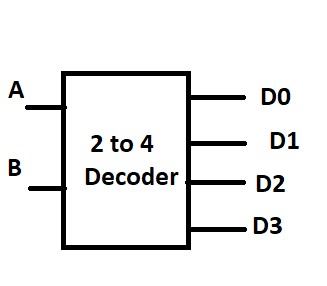
**Figure 5 - Encoder**

**Objectives**

* To understand the concept of active low and high enabling decoder
* To learn the importance of priority encoder
* To implement the priority encoder

**Lab Task # 1**

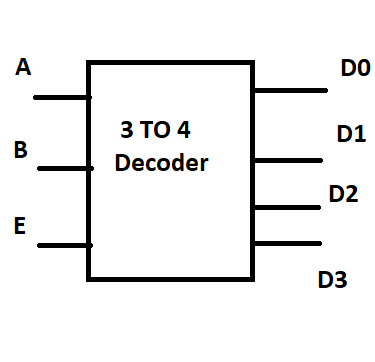
1. Draw block diagram of 2-to-4 line decoder.



1. Fill the table given below

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | **Outputs** | | | | |
| **A** | **B** | | **D0** | **D1** | **D2** | **D3** |
| 0 | 0 | | 1 | 0 | 0 | 0 |
| 0 | 1 | | 0 | 1 | 0 | 0 |
| 1 | 0 | | 0 | 0 | 1 | 0 |
| 1 | 1 | | 0 | 0 | 0 | 1 |

1. Write Boolean expressions (SOP) for each output.
2. Design the 2 to 4 line circuit diagram of decoderwith an additional enable input E.



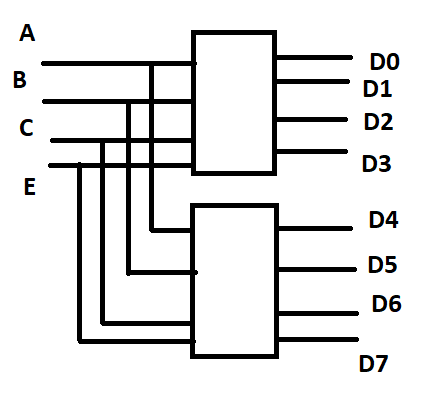
1. Implement the designed 2-to-4 line decoder on **Circuit Maker** and fill the given truth table below.

|  |
| --- |
| Circuit Maker Implementation |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | **Outputs** | | | |
| **E** | **A** | **B** | **D0** | **D1** | **D2** | **D3** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 |

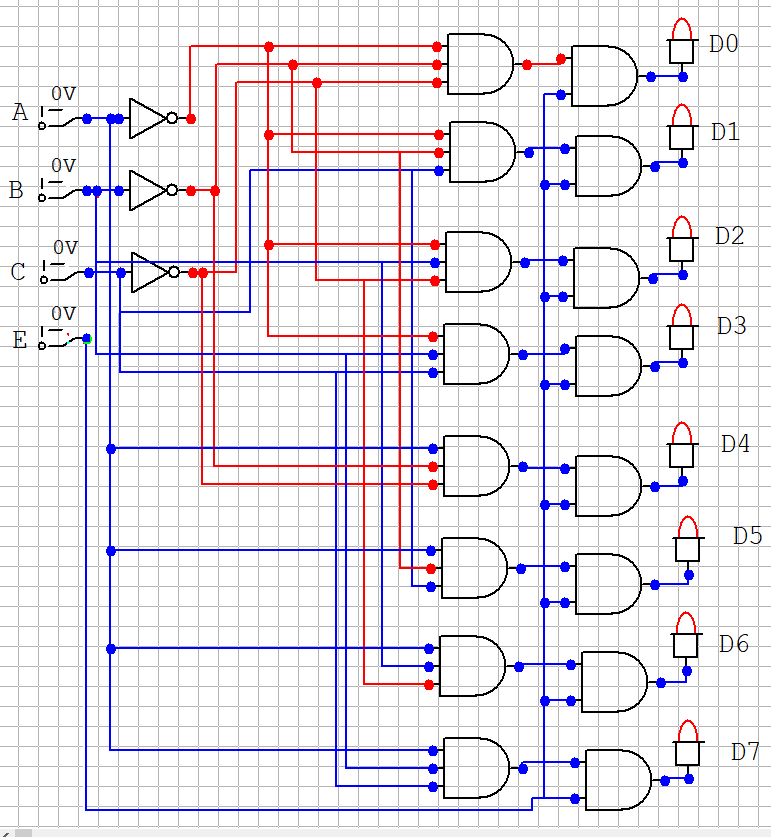
**Task # 2. Construct a 3-to-8 decoder using two 2-to-4 decoders with enable inputs.**

Hint. Draw block diagram, truth table, write corresponding Boolean expressions and finally implement circuit diagram.



|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | | **Outputs** | | | | | | | |
| **E** | **A** | **B** | **C** | **D0** | **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

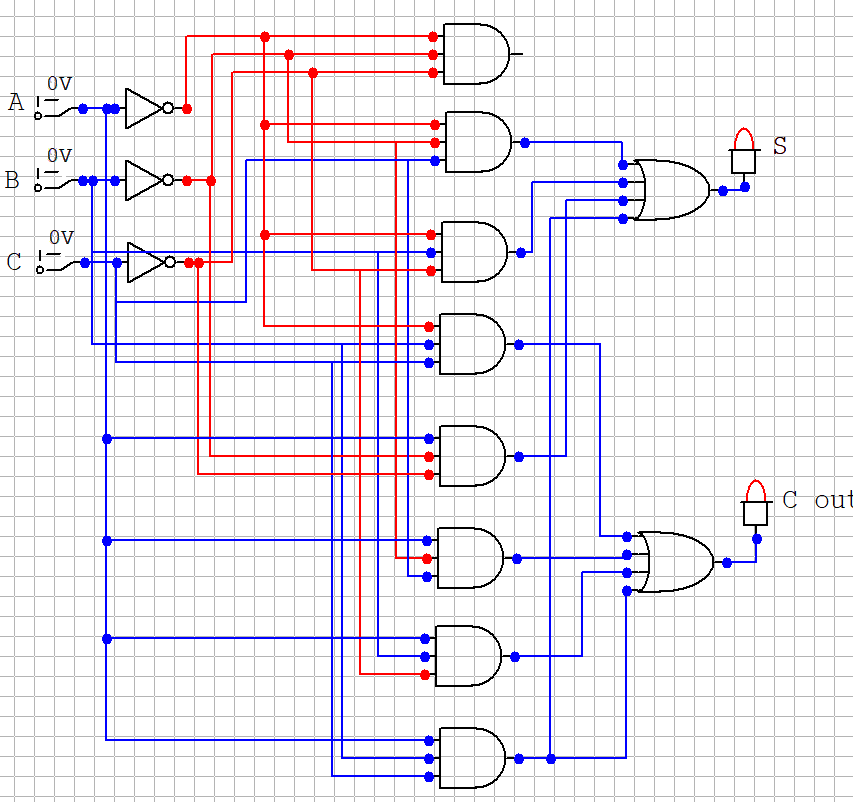
|  |  |
| --- | --- |
| Output | Expressions |
| D0 | E A’B’C’ |
| D1 | E A’B’C |
| D2 | E A’B C’ |
| D3 | E A’B C |
| D4 | E A B’C’ |
| D5 | E A B’C |
| D6 | E A B C’ |
| D7 | E A B C |



**Task # 3. Implementation Full Adder using 3-to-8 decoder**

Hint. Create truth table, write corresponding minterms and finally implement circuit diagram using decoder.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | Cin | S | Cout |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |



**Task # 4.** Design a robot motion navigation system using minimum control buttons. The robot can move forward, backward, left, right and stop (depending on the scenario). However, the robot is limited to take only one decision at a time.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | **Outputs** | | | | |
| **A** | **B** | | Left | Right | Up | Down |
| 0 | 0 | | 1 | 0 | 0 | 0 |
| 0 | 1 | | 0 | 1 | 0 | 0 |
| 1 | 0 | | 0 | 0 | 1 | 0 |
| 1 | 1 | | 0 | 0 | 0 | 1 |

**Task # 5. Design a 4-to-2 encoder.**

1. Table 1 given below is for 4-input **encoder**.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Table 1: Truth Table of 4-input encoder | | | | | |
| Inputs | | | | Outputs | |
| D3 | D2 | D1 | D0 | B | A |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 |

1. The simplified Boolean expression for Aand B are.
2. Draw a combine circuit diagram **on Circuit Maker** for the above Boolean expressions A and B and fill the table 2 given below.

|  |
| --- |
| **Circuit Maker Implementation** |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Table 2: Truth Table of 4-input encoder | | | | | |
| Inputs | | | | Outputs | |
| D3 | D2 | D1 | D0 | B | A |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 |

1. Test your encoder for the following inputs given in table 3 and Fill the table 3.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Table 3: Truth Table of 4-input encoder | | | | | |
| Inputs | | | | Outputs | |
| D3 | D2 | D1 | D0 | B | A |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |

1. Did you find the error? Check table 3 and 2 for the corresponding inputs. Please comment below your understanding.
2. If there is any error how can we correct it? Please comment below and discuss.